

February 22, 2002

To: Commissioner of Patents and Trademarks

Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572

20 McIntosh Drive

Poughkeepsie, N.Y. 12603

TO 12000 -

Subject:

Serial No. 10/036,898 01/04/02

Shao Yen Ku

A SUCCESSFUL AND EASY METHOD TO REMOVE POLYSILICON FILM

Grp. Art Unit: 1765

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 27, 2002.

Stephen B. Ackerman, Req.# 37761

Signature/Date Stephen Backery 2/27/02

TSMC-01-380

- U.S. Patent 5,928,969 to Li et al., "Method for Controlled Selective Polysilicon Etching," describes a method for controlled selective polysilicon etching employing an NH4OH plus NH4F polysilicon etch and a hemispherical grain (HSG) polysilicon process.
- U.S. Patent 6,100,203 to Kil et al., "Methods of Employing Aqueous Cleaning Compositions in Manufacturing Microelectronic Device," describes a polysilicon etch and subsequent aqueous cleaning composition cleaner methods.
- U.S. Patent 5,431,777 to Austin et al., "Methods and Compositions for the Selective Etching of Silicon," describes methods and compositions for the selective etching of silicon.
- U.S. Patent 5,296,093 to Szwejkowski et al., "Process for Removal of Residues Remaining After Etching Polysilicon Layer in Formation of Integrated Circuit Structure," describes a process for removal of residues remaining after etching a polysilicon layer.
- U.S. Patent 5,030,590 to Amini et al., "Process for Etching Polysilicon Layer in Formation of Integrated Circuit Structure," describes a process for etching a polysilicon layer in the formation of an integrated circuit structure.

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- U.S. Patent 4,113,551 to Bassous et al., "Polycrystalline Silicon Etching with Tetramethylammonium Hydroxide," describes a method for polycrystalline silicon etching with tetramethylammonium hydroxide.
- U.S. Patent 5,963,804 to Figura et al., "Method of Making a Doped Silicon Structure with Impression Image on Opposing Roughened Surfaces," describes a method of making a doped silicon structure with an impression image on opposing roughened surfaces.
- U.S. Patent 5,976,767 to Li, "Ammonium Hydroxide Etch of Photoresist Masked Silicon," describes a process for selectively removing silicon containing material using an ammonium hydroxide etch.

Sincerely,

Stephen 3 Cickernu-Stephen B. Ackerman,

Req. No. 37761

EXAMMER

Binh Tran

DATE CONMIDERED

5/4/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.